Form 1449*	Atty. Docket No.: 303.586US1	Serial No. 09/320,421
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U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No

OTHER DOCUMENTS

**Examiner Initial	(Including Author, Title, Date, Pertinent Pages, Etc.)
GT	Blalock, T.N., et al., "A High-Speed Sensing Scheme for 1T Dynamic RAM's Utilizing the Clamped Bit-Line Sense Amplifier", IEEE Journal of Solid-State Circuits, 27(4), pp. 618-625, (April 1992)
GT	Kuge, S., et al., "SOI-DRAM Circuit Technologies for Low Power High Speed Multigiga Scale Memories", IEEE Journal of Solid-State Circuits, 31(4), pp. 586-591, (April 1996)
GT	Parke, S.A., "Optimization of DRAM Sense Amplifiers for the Gigabit Era", IEEE, Proceedings of the 40th Midwest Symposium on Circuits and Systems, Sacramento, CA, pp. 209-212, (1997)
GT	Suma, K., et al., "An SOI-DRAM with Wide Operating Voltage Range by CMOS/SIMOX Technology", IEEE Journal of Solid-State Circuits, 29(11), pp. 1323-1329, (November 1994)

Examiner	Date Considered
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*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.